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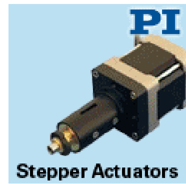


Recent Editorial

## MICRO/NANO TECHNOLOGY
## Advancing electronic packaging, one solder joint at a time

**Cemel Basaran (l) and Alexander Cartwright use the Electronic Packaging Lab's moire interferometry unit to detect nanoscale solder-joint strain. (Photo: Univ. of Buffalo)**

The activity within microelectronics has centered around two main problems: 1) making IC's faster and 2) creating smaller, more reliable packaging. A group from the Univ. of Buffalo, N.Y., headed by Cemal Basaran and Alexander Cartwright, are addressing these issues by targeting solder joints as a field for innovation. These areaswhere the circuits are fused onto a boardare known to be susceptible to high current densities and temperature, which causes them to degrade over time.

"Solder joints are the biggest bottleneck and source of failure in microelectronics," says Cartwright. "The chip themselves don't fail; it's where the chips interact on the board that the failure occurs." This has led the team to create a method to measure the amount of damage done to the package during thermal and vibrational loading, when there is high current.

According to Basaran, the team has "developed a technique to survey this strain on a nanoscale and in real-time, with a displacement resolution down to 27 nm." This data was then used to create computer models, which have now given the team, along with vendors such as Intel, insight into how to prevent these failures.

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