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Friday 29 May 2009

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### US researchers warn chip makers over solder stress

Wednesday 24 September 2003

#### US researchers warn chip makers over solder stress Steve Bush

Future microprocessors will have to go Pb-free if electromigration is not to ruin in-package and package to PCB solder joints, claims the University at Buffalo.

The problems exist at current densities of 10<sup>5</sup> to 10<sup>6</sup> A/cm<sup>2</sup>. "This may seem high, but if you make a 25µm joint in a 10GHz processor, this is what you get," Dr Cemal Basaran, director of Buffalo's Electronics Packaging Laboratory told Electronics Weekly. "The total power that this [future] device needs is probably less than a Pentium 4, but the power density is going up."

Flip-chip-mounted microprocessors and ball-grid array power components - there are no flip-chip power components - are most vulnerable, he said.

The Buffalo team has used laser Moiré interferometry to measure stress and strain in sectioned solder joints while they are subjected to weeks of high current abuse. Deflections down to 27nm are detectable.

"No one else in the world is doing what we're doing," said Basaran.

Careful experimental work has removed thermal effects, narrowing joint deterioration to electromigration, and particularly the electromigration of Pb. "Lead migrates very, very quickly," said Basaran. "Lead-free is definitely better than tin-lead. Tin-silver-copper, for instance, is much more resistant."

Electromigration causes the solder material to shift, leaving voids, said Buffalo. Too many voids force current to find new paths, or electrons become trapped between voids within the solder. "Anytime you have defects, it accelerates a breakdown of the package and soon you have failure," said lab co-director Alexander Cartwright.

Alongside its practical work, the lab has developed theoretical models which are now agreeing with actual joints. "With the computer models, we can design a complete system without having to build more than one prototype," Basaran says.

[www.packaging.buffalo.edu](http://www.packaging.buffalo.edu) Wavelet-enhanced Moiré interferometry The Buffalo team uses phase-shifted Moiré interferometry to make its measurements.

The basic Moiré technique used has a resolution of 417nm per fringe which is boosted to 27.8nm/fringe by carefully analysing phase.

"Specifically, a one-dimensional continuous wavelet transform technique was developed to effectively reduce the transient environmentally induced noise and the static background noise that complicates phase determination," said researcher Heng Liu in a paper on measurement enhancement.

Relative phase shifts in the interferometer pictures were measured to within two per cent using wavelet transforms.

A solder joint between copper conductors. The bottom view showing Moiré fringes is after several weeks of high current. This is a Pb-free joint which stabilised in this state after around 700 hours.

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