Failure Modes of Flip Chip Solder Joints Under High Electric Current Density

The failure modes of flip chip solder joints under high electrical current density are studied experimentally. Three different failure modes are reported. Only one of the failure modes is caused by the combined effect of electromigration and thermomigration, where void nucleation and growth contribute to the ultimate failure of the module. The Ni under bump metallization–solder joint interface is found to be the favorite site for void nucleation and growth. The effect of pre-existing voids on the failure mechanism of a solder joint is also investigated [DOI: 10.1115/1.1898338]

Keywords: Flip Chip, Solder Joint Reliability, Electromigration, Thermomigration, Current Stressing, High Current Density, Power Electronics, Nanoelectronics

1 Introduction

Electromigration in solder joints under high direct current density is known as a reliability concern for the future high density microelectronic packaging and power electronic packaging [1–7]. The trend in flip-chip to increase I/O count drives the interconnecting solder joints to be smaller in size and, thus, carry higher current density. The current density will increase further as chip voltage decrease and absolute current levels increase. The research on electromigration and thermomigration in solder joints is still in its early stages, hence the literature is very poor in publicly available data. The failure modes of flip-chip solder joints under high electric current stressing are not yet well understood. In the experiments, 20 test vehicles flip chip modules were subjected to dc electric current stressing. The stressing current level ranges from 0.5 to 1.5 A and leads to a current density in the solder joint from 0.4 to 1.2 × 10^4 A/cm^2 dependent on the cross-sectional area of solder joint. Two test modules were subjected to dc pulse current stressing at a level of 3–10 A. 14 test modules failed due to current stressing; 4 test modules were damaged due to re-polishing after the nano-indentation tests; 2 test modules survived more than 3000 h of stressing. Table 1 shows the test vehicle number and applied current levels for each module tested.

2 Experimental Setup

The test vehicle flip chip modules were provided by Motorola Corp. The test module has a dummy silicon die with only aluminum (Al) conductor trace on it. The silicon die is attached on a FR4 printed circuit board (PCB) through eutectic Pb37/Sn63 solder joints. The copper plates on the PCB provide the wetting surface for the solder joints. The under bump metallization (UBM) on silicon die side is electroless Ni. The voids between the solder joints are filled with underfill between the silicon die and PCB substrate. The thickness of the Al trace is about 1 μm and the width is about 150 μm. The height of the solder joint is 100 μm. The test module was cross sectioned and finely polished toward the center of the solder joints before current stressing.

On each module, two solder joints were tested. The solder joints on each test module are named in such a way that current stressing happens at the center of the solder joints before current stressing. The trend in flip-chip to increase I/O count drives the interconnecting solder joints to be smaller in size and, thus, carry higher current density. For M31 and M33, electromigration and thermomigration should have no contribution to the failure of the module. M53 survived just 22.5 h of current stressing. The initial stressing temperature measured on Si die was 150°C then gradually increased over 180°C. M31 and M33 failed after 30 min of current stressing with a measured Si die temperature of over 200°C. The solder joints in these two test modules melted (Fig. 2). The joule heating heat was apparently generated in the Al trace since the solder joint has good wetting with both Ni UBM on the Si die side and Cu plate on the FR4 side. Therefore, Al trace contributed to most of the resistance. For M31 and M33, electromigration and thermomigration should have no contribution to the failure of the module. M53 survived just 22.5 h of current stressing. The initial stressing temperature measured on Si die is 150°C then gradually increased over 180°C.

M4, M5, M7, and M54 exhibited type 2 failure, among which M4 and M7 were subjected to pulsed direct current (PDC) stressing. Tektronix® 371 A curve tracer was used for pulse stressing. The pulse frequency is 120 Hz with a pulse width of ~80 μs. Pulse shape depends on the wiring impedance, but resembles a rectangular wave. The duty factor (defined as the ratio of time of the on-period to that of the whole pulse period) is calculated to be 0.96%. When M4 was subjected to 10 A peak PDC stressing, its resistance increased to infinity immediately. SEM image shows that the damage of the module was in the Al trace and silicon die as clearly shown in Fig. 3(a). M7 was first subjected to 3 A of PDC stressing for 50 h, then 5 A of PDC stressing for 57 h, and...
finally 7 A of PDC stressing for 23 h. SEM images taken after stressing show that there was no microstructural change in the solder joints at all. When M7 was subjected to 10 A of PDC stressing, it failed immediately. Figure 3(b) shows that the Al trace was the actual failure cause of the module.

With 7 A of PDC, the peak current density in the solder joints was $5-7 \times 10^4$ A/cm$^2$, which is much higher than that applied in the dc current stressing experiments. The effect of PDC on electromigration has been shown to be dependent on the frequency and duty factor [8]. At low frequency electromigration acts as if it were dc for the time “on” and backdiffusion may occur during the time “off” [9]. In our experiment, the PDC frequency is within the low frequency regime. The reason that we did not observe any damage in the solder joint during PDC stressing when very high current density was applied may be due to the low duty factor ($0.96\%$) of PDC. On the other hand, high peak current of PDC generates a lot of heat in the Al trace which leads to its failure when 10 A PDC was applied.

M5 and M54 also experienced type 2 failure although they were subjected to dc stressing. For example, the applied current on M5 was 1.5 A and the module immediately failed. SEM secondary images of the solder joint B before and after stressing are shown in Fig. 4: Figure 4(b) shows that Si die separated from the solder joint and underfill along the Al trace where tremendous heat was generated.

Modules M6, M14, M34, M41, M42, M51, and M56 experienced type 3 failure. This mode of failure happened due to void nucleation and growth in the solder joint under current stressing. In the modules that experienced type 3 failure severe void nucleation was observed in the solder joints (Fig. 5). The fact that void nucleation was always on Si die side and mass accumulation on the Cu plate side on the cross-sectioned solder surface indicates that the failure process in solder joint is the combined effect of electromigration and thermo-migration [5]. In these modules, solder joint A (where the direction of electromigration is the same as that of thermomigration) always had much more severe void nucleation than solder joint B (where the direction of electromigration is opposite to that of thermo-migration). Therefore, the degradation of solder joint A caused the ultimate failure of the module.

4 Voids Nucleation in Solder Joints

To understand type 3 failure (which is due to mass migration, both electro and thermo), it is important to analyze the void nucleation modes in solder joints during current stressing and their relationship with the failure of these test modules. Besides the modules that experienced type 3 failure, there were other modules which also underwent void nucleation but never failed after 3000 h, when the test was terminated. We will discuss the void nucleation modes in all these modules. Four void nucleation modes were observed in these solder joints: mode (1) voids nucleate and grow in the Ni under bump metallization (UBM)-solder

<table>
<thead>
<tr>
<th>Current level</th>
<th>Test module</th>
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<tbody>
<tr>
<td>0.5A</td>
<td>M8, M15, M26</td>
</tr>
<tr>
<td>1A</td>
<td>M1, M6, M12, M14, M22, M31, M33, M41, M42, M51, M52, M54, M56</td>
</tr>
<tr>
<td>0.9A</td>
<td>M34</td>
</tr>
<tr>
<td>1.15A &amp; 1.5 A</td>
<td>M5, M53</td>
</tr>
<tr>
<td>Pulse</td>
<td>M4, M7</td>
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</tbody>
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Fig. 1 Schematic cross section of the test vehicle module

Fig. 2 Secondary SEM of M33 after failure: solder joint B

Fig. 3 Failure in the Al trace and Si die, (a) M4, solder joint A, (b) M7, solder joint A

Table 1 Test matrix of flip chip modules
interface; (2) voids nucleate and grow in the region near Ni UBM–solder interface; (3) growth of pre-existing voids; (4) no void growth after 3000 h of testing. Table 2 provides mode of void growth for the test vehicles. Some of the modules listed in the table experienced void nucleation and growth, but their failure was due to polishing after nano indentation.

For mode 1 voids were observed to nucleate and grow on the Ni UBM–solder interface for the majority of the solder joints. This interface was the favorite site for void nucleation and growth. The combined electromigration and thermomigration effect leads to an atomic flux divergence in this region for both solder joints A and B (meaning the depletion of mass in the region) since Ni UBM acts as a barrier layer for the diffusion of solder joint. The direction of overall diffusion due to the combined effect of thermomigration and electro-migration is from Ni UBM–solder interface to Cu plate in both solder joints A and B as reported by Ye et al. [5]. Theoretical electromigration analysis indicates that maximum tensile spherical stress will be generated in this region and vacancy condensation will also occur in this region \[10–20\]. The driving force for void nucleation and growth is proportional to the tensile stress \[21\]. Gleixner and Nix [22] numerically calculated the void nucleation rate in passivated interconnect line due to electromigration and thermal stress based on vacancy condensation theory \[23,24\], and suggested that void nucleation due to vacancy condensation is extremely slow and would not be expected to occur in reality. Flinn [25] proposed the possibility of contaminants at the metal/passivation interface acting as void nucleation sites in passivated metal lines. Gleixner and Nix [22] analyzed the effect of contaminants on void nucleation and found that void formation at a flaw at the interface would require a considerably smaller stress than that in classical void nucleation theory. They further concluded that voids would grow only at the intersection of the grain boundary with the passivation layer due to the large difference between the grain boundary and lattice diffusivities. For void growth to occur atoms must be removed from the void surface and grain boundary acts as an extremely fast path for material removal relative to the lattice \[22\]. Raj [26] showed that heterogeneous nucleation at the triple junction of a second phase particle and a grain boundary was the most probable. Based upon the above-presented discussion, it is clear that the Ni UBM–solder interface is the naturally preferable site for voids nucleation and growth, as observed in our experiments. The voids would nucleate at the interface of Ni layer–solder joint intermetallic compound. Contaminants lodged in this interface during manufacturing process make this site a preferred location for void nucleation. This interface has the maximum atomic divergence which is favorable for void growth. Figures 6 and 7 show examples of mode 1 void nucleation and growth on the Ni UBM–solder joint interface.

### Table 2 Summary of voids nucleation and growth modes in the experiments

<table>
<thead>
<tr>
<th>Voids nucleation and growth mode</th>
<th>Mode 1</th>
<th>Mode 2</th>
<th>Mode 3</th>
<th>Mode 4</th>
</tr>
</thead>
</table>
Only three solder joints were observed to have mode 2 void nucleation and growth. Figure 8(a) shows the void nucleation in the region near Ni UBM—solder joint interface in M34, solder joint A after 268 h of current stressing. Hillocks were observed to build up near the solder–Cu plate interface. Figure 8(b) shows void growth and development of severe depression in the region near the Ni UBM–solder interface after 444 h of current stressing. One unexpected observation is that new voids nucleated in the region of hillocks. The origin of these new voids is not clear, since they were in the downwind region of thermomigration and electromigration, where atoms diffuse into and the material experiences compressive stress. Hence the theory of void nucleation and growth under tensile hydrostatic stress does not apply in this region. One possibility for this behavior is void nucleation and growth under shear stress. Xue et al. [27] reported that the shear bands are the preferred sites for nucleation, growth, and coalescence of voids and are, as such, precursors to failure in titanium and Ti-6Al-4V alloy. In the hillocks region of solder joint A in M34, the material was subjected to biaxial compression stress according to electromigration theory, but in the direction perpendicular to the solder surface the normal stress is zero. Therefore, the material in this region is also subjected to shear stress and this might be the cause of new void nucleation.

Voids nucleated in the hillocks regions later become smaller after further current stressing. This probably indicates that after the voids in the hillocks region nucleate and grow to a certain extent, the stresses triggering this void growth in this region are counterbalanced by mass accumulation. Since the hillocks region is where the atoms diffuse into, the healing of the previous voids was observed. On the other hand, the depression near the UBM–solder interface continued to grow. The SEM image after the failure indicates that the direct cause of failure was the severe depression and voids growth in the UBM–solder interface region. It is worth noting that M34, solder joint A was the only solder joint to be found void of nucleation in the hillocks region among all the modules we tested. Voids nucleation and growth in the region near Ni UBM–solder interface was also found in solder joint B of M41 and solder joint B of M56. But they were much less severe compared to solder joint A of M34 because the direction of thermomigration is opposite to that of electromigration in these solder joints. Of all the solder joints that were tested, only three solder joints had mode 2 void nucleation and growth behavior, indicating voids nucleation in the region near UBM–solder interface is less favorable than that on the UBM–solder interface itself.

Some of the solder joints we tested had pre-existing voids. These pre-existing voids are generally produced during the reflowing process. Some of these pre-existing voids lead to mode 3 void growth where the growth of pre-existing voids causes the ultimate failure of the test module. According to our experiment results, whether or not these pre-existing voids would grow or not depends on their locations: if the pre-existing voids are located in the region near Ni UBM–solder interface where atoms diffuse out due to the combined effects of thermomigration and electromigration, they are likely to grow; if the voids are not located in UBM–solder interface region, they are very unlikely to grow.

This observation is best presented in Fig. 9. As shown in Fig. 9(a), there were several pre-existing voids as seen on the cross-sectioned surface of solder joint A of module M56. One small void with irregular shape was located in the region near UBM–solder interface; and several others were located near Cu–solder interface, two of them with round shape and others with irregular shape. It is clearly shown in Fig. 9(b) that only the pre-existing
void in the region near UBM–solder interface grew dramatically to form a big crack in that area. On the other hand, other bigger voids near Cu–solder interface did not grow very much, no matter what their initial shapes were. Yet, they did change their shape a little bit possibly due to the local stress build up and local surface diffusion. This observation agrees with Lee et al.1 findings. Figure 9 shows that besides severe void growth in the region near UBM–solder joint interface, two hillocks were gradually built up on the surface and a depression area was formed between these two hillocks.

This observation indicates that the diffusion process was not homogeneous within the solder joint. Careful examination of the phase structure reveals that the Pb-rich phase in the depression region was not equiaxially shaped and had a preferred orientation compared to that in hillocks regions as shown in Fig. 10. This preferred Pb phase orientation was formed during manufacturing and was preserved during current stressing. According to Kwok and Ho [28], the effective boundary diffusion coefficient, \( D_a \), equals \( \delta D_{gb}/d \), where \( \delta \) is the grain boundary width, \( D_{gb} \) is the grain boundary diffusivity, and \( d \) is the average grain size. Although the Pb phase size is not the actual grain size, there ought to be a proportional relationship between this phase size and grain size; the larger the phase size, the larger the grain size. The orientation in-equiaxed phase structure indicates an orientation in-equiaxed grain structure, which leads to the difference of average grain size in different directions. This means the effective diffusivity may not be isotropic in this region, and therefore the diffusivity in the whole solder joint is inhomogeneous. The observation suggests that the phase structure of eutectic Sn/Pb solder joint affect its diffusion property and therefore, the failure process under current stressing.

Figure 11 shows another example of the growth of pre-existing voids. The pre-existing voids in solder joint A of M41 were located very near to the Ni UBM–solder interface and were produced during manufacturing. The pre-existing voids were observed to grow rapidly toward the UBM–solder interface and lead to the ultimate failure of the module as shown in Fig. 12.

Among the modules that were tested, some of them never experienced voids nucleation and growth after 3000 h of current stressing as shown in Table 2.

M8, M15, and M26 were all subjected to 0.5 A of dc current stressing. Relatively low current level leads to relatively low current density in the solder joints as well as smaller joule heating.
models resulted from Joule heating and lack of cooling in the specimen. These failure modes happen very quickly and influence of electromigration and thermomigration is negligible. Most of the modules experienced combined electromigration and thermomigration induced failure. In this mode of failure, thermomigration significantly dominates the failure process. When the direction of the thermomigration is the same as the electromigration the damage is severe. When the direction of the electromigration and thermomigration are opposite the thermomigration forces dominate yet the total damage is smaller. The Ni UBM–solder joint interface was the preferred site of the void nucleation and growth. It is believed that the contaminants in the interface also accelerate the void nucleation process. The effect of pre-existing voids on the failure process of a solder joint is found to be dependent on their location.

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References


